ECTE 432 Project 2: MIPS PIPELINE

Done by:

Edwin Dsouza

6279570

GitHub Link: [ed722uowd/432-project-2 (github.com)](https://github.com/ed722uowd/432-project-2)

Contents

[Simulink Circuit: 2](#_Toc90070122)

[Waveforms: 2](#_Toc90070123)

[First Branch: 7](#_Toc90070124)

[Last High of Mem Write: 7](#_Toc90070125)

[The use of multiple delays for testing: 8](#_Toc90070126)

# Simulink Circuit:

Diagram

Description automatically generated

Figure 1. MIPS Pipeline Structure

# Waveforms:

Waveforms in increments of 32 clock cycles.

Graphical user interface, application

Description automatically generated

Figure . Overall Waveform

Graphical user interface

Description automatically generated

Figure . Clock Cycle 0 - 32

A screenshot of a computer

Description automatically generated with medium confidence

Figure . Clock Cycle 32 - 64

Graphical user interface

Description automatically generated

Figure . Clock Cycle 64 -96

A screenshot of a computer

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Figure . Clock Cycle 96 -128

A screenshot of a computer

Description automatically generated with medium confidence

Figure . Clock Cycle 128 - 160

Graphical user interface

Description automatically generated

Figure . Clock Cycle 128 - 192

Graphical user interface

Description automatically generated

Figure Clock Cycle 192 - 224

Graphical user interface

Description automatically generated with medium confidence

Figure . Clock Cycle 220 -250

# First Branch:

Graphical user interface

Description automatically generated

Figure . First Branch

The waveform branches to the 8th instruction at the 44th clock cycle

# Last High of Mem Write:

A screenshot of a computer

Description automatically generated with medium confidence

Figure . Last Mem Write high and Write data to data memory

Last high of Mem Write happens at the 156th clock cycle with the data written to memory being 30.

# The use of multiple delays for testing:

The waveform for a particular output wouldn’t come when taken after a buffer (comprised of delay and register block). In order to deal with this, it was decided to use a delay block to delay the output till the Mem Stage. For instance, the PC counter had issues when trying to add it to the waveform viewer when taken from the EXE stage. To align the PC at the MEM stage a delay of 6 clock cycles was added to the PC at the fetch stage, since it had to traverse through 3 buffers each with a delay count of 2.

To confirm the working of the model, all waveforms were analyzed in the MEM stage using delay units in some cases.